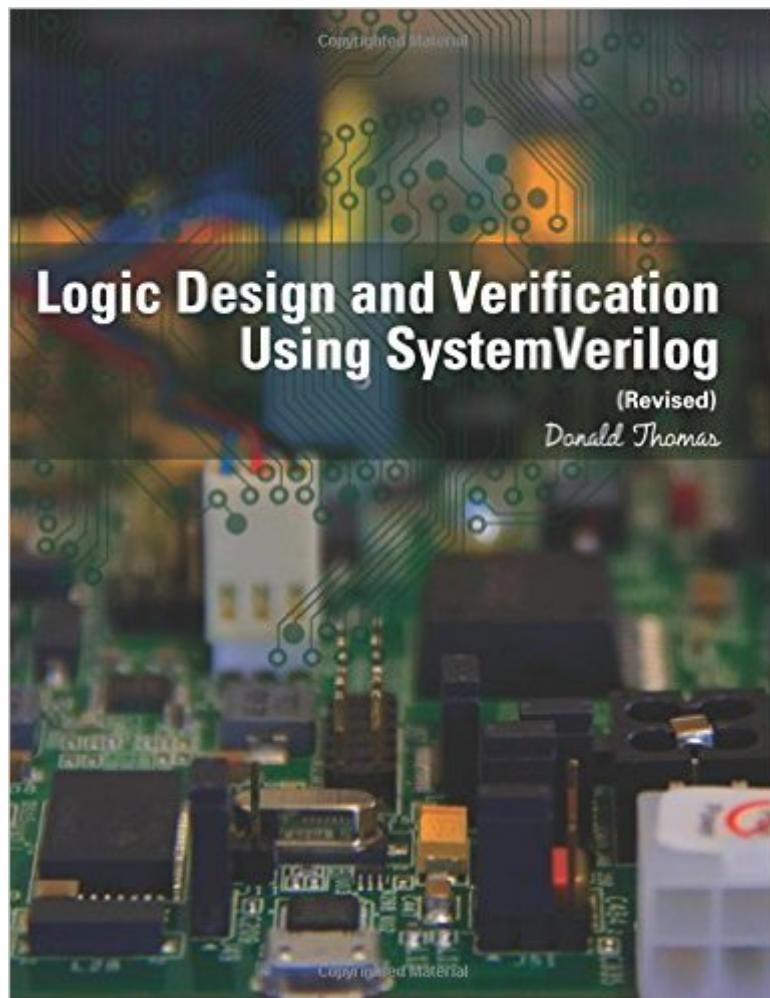


The book was found

Logic Design And Verification Using SystemVerilog (Revised)



Synopsis

SystemVerilog is a Hardware Description Language that enables designers to work at the higher levels of logic design abstractions that match the increased complexity of current day integrated circuit and field-programmable gate array (FPGA) designs. The majority of the book assumes a basic background in logic design and software programming concepts. It is directed at: ¢ students currently in an introductory logic design course that also teaches SystemVerilog, ¢ designers who want to update their skills from Verilog or VHDL, and ¢ students in VLSI design and advanced logic design courses that include verification as well as design topics. The book starts with a tutorial introduction on hardware description languages and simulation. It proceeds to the register-transfer design topics of combinational and finite state machine (FSM) design ¢ these mirror the topics of introductory logic design courses. The book covers the design of FSM-datapath designs and their interfaces, including SystemVerilog interfaces. Then it covers the more advanced topics of writing testbenches including using assertions and functional coverage. A comprehensive index provides easy access to the book's topics. The goal of the book is to introduce the broad spectrum of features in the language in a way that complements introductory and advanced logic design and verification courses, and then provides a basis for further learning. Solutions to problems at the end of chapters, and text copies of the SystemVerilog examples are available from the author as described in the Preface.

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Customer Reviews

This is a really great book, covering a significant gap in most curriculum: whatever happens after the intro digital logic class. This book takes your SystemVerilog skills to the next level. Most significant

digital systems will have many interacting, cooperative FSMs. How do you design for cooperation? How do you interface them together? And, most importantly, how do you test them as a system? These are the major themes of this book. Specific topics include: interfaces, hardware threads, interactions among those thread (synchronous and asynchronously), testbenches, randomization in the testbench, concurrent assertions, and measuring functional coverage. The book also presents a deep model of the simulation kernel, showing what it does during the many different phases of each simulation cycle. You'll always be able to answer the questions about why your testbench needs "

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